VOLTAGE CONTROLLED QUADRATURE OSCILLATOR WITH PHASE TUNING

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5   **BACKGROUND OF THE INVENTION**

Field of the Invention

The present invention relates to the field of ring oscillators and more particularly to phase tuning of a ring oscillator and to the use of a phase tuning ring oscillator in an image reject mixer.

10   **Description of the Related Art**

Frequency divide-by-two circuits that are based on analog injection locking techniques to perform frequency division are known as frequency halvers or regenerative dividers.

Figure 1, labeled prior art, illustrates a block diagram of a frequency halving circuit

15   100 as presented in "*RF analog and digital circuits in SiGe technology*", J.R. Long, M. Copeland, S. Kovacic, D. Malhi and D. Harame, Proceedings of the ISSCC, San Francisco CA, pp. 82-83, February 1996. Differential amplifiers 102 and 104 are connected to form a ring oscillator. A differential AC current source 112 is connected across emitter-coupled nodes 114 and 116 of differential amplifiers 102 and 104. Differential AC current source 112

20   is set at a frequency ($2f_{LO}$) that is twice the fundamental frequency (f_{LO}) of the ring oscillator. This causes the doubled-frequency emitter-coupled node voltages of the ring oscillator to become synchronized to the injected currents of I_{inj} from differential AC current source 112. An important feature of frequency halving circuit 100 is that emitter-coupled $2f_{LO}$ input signal injection is symmetric with respect to the topology of the ring oscillator because the

25   injected currents affect both amplifying stages 102 and 104 of the ring oscillator identically. The result of this symmetry is that the outputs V_1 and V_Q remain in precise phase quadrature for the entire locking range of the ring oscillator, not just at the center (or free-running) frequency of the ring oscillator. In practice, this can be achieved with a phase error on the

order of < 1°. The frequency of the quadrature outputs V_I and V_Q are half that of the injected current and so frequency halving circuit 100 performs a frequency divide-by-two (or halving) function.

In radio system architectures, image reject mixing requires accurate quadrature local

5   oscillator signal generators to attain high image rejection performance. This is required for both up (transmitter) and down (receiver) conversions. Known designs attempt to design the quadrature signal generator (frequency divider) to produce as accurately as possible a pair of signals (generally referred to as the inphase (I) and quadrature (Q) signals) which are separated by precisely 90°. It is difficult to account for all process tolerances which can

10 impair the image rejection performance of an image reject architecture. Approximately 1° of phase error is common. This translates to a maximum image rejection of about 46 dB. Including other sources of phase and amplitude error in the quadrature down conversion path a typical specification for image rejection is approximately 35 dB. In order to improve image rejection beyond this level, a system is required for controlling the phase relation between the

15 I and Q local oscillator signals with a high degree of precision. Such a system could be used to provide I and Q signals which have a phase relation which compensates for the other sources of phase error. In a particular case, the phase relation between the I and Q signals may be greater or less than 90°.

Figure 1B, labeled prior art, illustrates a conventional front-end topology 120

20 commonly used in high-performance receiver front-ends. Radio frequency (RF) signal 130 includes both a desired RF band and an unwanted image band which are converted to the same intermediate frequency (IF) band because they share the same frequency separation from the local oscillator (LO) carrier. Discrete filters, including preselect filter 142 and image reject filter 144, are used to suppress the unwanted image band. A total image

25 rejection (IR) on the order of 70-100 dB is typically required. Preselect filter 142 band-limits RF signal 130 to prevent out-of-band carriers from desensitizing or overloading a low noise amplifier (LNA) 150. Preselect filter 142 also provides some image rejection, typically on the order of 30 dB, if the image band is outside the pass-band of preselect filter 142. The rest of the image rejection is obtained by a second off-chip filter, image reject filter 144, placed

30 between LNA 150 and a mixer 160. Image reject filter 144 is typically more aggressive than preselect filter 142 (approximately 45 dB image rejection) and has a higher insertion loss

-2-

799110 v3

(approximately 3-4 dB). Placing image reject filter 144 after LNA 150 reduces the effect of insertion loss on the noise figure of the receiver.

Topology 120 works well for many low-cost implementations. However in an integrated receiver integrated circuit (IC) application, performance is compromised by having

5 to route RF signal 130 through an off-chip filter, i.e., image reject filter 144. Wideband 50Ω matching networks are required at the RF interfaces to the integrated circuit, causing the signal to be filtered to suffer board, package, and filter losses before being sent back on-chip to drive the mixer. Multi-chip modules with controlled impedance packages reduce parasitics and losses but not power consumption and add significant cost. Furthermore, fixed-frequency

10 discrete RF filters limit system flexibility in an open standard environment.

Figure 1C, labeled prior art, illustrates a block diagram of an image reject mixer 170 using the Hartley topology described in U.S. Patent No. 1,666,206, Apr. 1928, R. Hartley, *"Single-sideband modulator,"* and *"A third method of generation and detection of single sideband signals,"* D.K. Weaver, Proceedings of the IRE, vol. 44, pp. 1703-1705, 1956.

15 Signal RF_{in} comprises a RF signal having a frequency f_{RF} and an image signal having a frequency f_{IM}. Signal generator 171 provides a pair of local oscillator signals V_1 (referred to as the in-phase or 0° signal) and V_2 (referred to as the quadrature or 90° signal), both having the same frequency f_{LO}. Signals V_1 and V_2 have phase angles ϕ_{V1} and ϕ_{V2}. ϕ_{V1} is arbitrarily chosen as a reference for 0° phase. Signals V_1 and V_2 are mixed with the received signal RF_{in}

20 in mixers 172 and 174 to provide a pair of signals IF_1 and IF_2. When high side injection is used (f_{LO} is greater than f_{RF}), the IF_1 signal comprises the RF signal converted to frequency ($f_{LO} - f_{RF}$) and the image signal (sideband) converted to frequency ($f_{IM} - f_{LO}$). Signal IF_2 comprises the RF signal converted to frequency ($f_{LO} - f_{RF}$) and shifted in phase by $\phi_{V2}°$ and the image signal converted to frequency ($f_{IM} - f_{LO}$) and shifted in phase by $-\phi_{V2}°$.

25 The amplified signals IF_1 and IF_2 are combined by a quadrature combiner 180. Quadrature combiner 180 is designed to complete the image rejection by providing a phase shift ϕ_{QC1} to signal IF_1 and a phase shift ϕ_{QC2} to signal IF_2. Ideally, to maximize suppression of the image signal, $\phi_{QC1} - \phi_{V1} = 0°$ and $\phi_{QC2} + \phi_{V2} = -180°$ (assuming high side injection). Ideally, $\phi_{V2} - \phi_{V1} = 90°$, $\phi_{QC2} - \phi_{QC1} = 90°$. In known quadrature combiners, $\phi_{QC2} - \phi_{QC1}$ is

30 generally not 90°. Typically a phase error exists, and the image is not maximally suppressed.

In addition, known quadrature combiners also introduce amplitude errors in the IF_1 and/or IF_2 signal paths. For example, signal IF_1 can be reduced in amplitude by N dB.

Current state of the art systems attempt to maintain the 90° phase separations between ϕ_{V1} and ϕ_{V2} and between ϕ_{QC1} and ϕ_{QC2}. It has been found that image rejection performance

5 can be substantially increased by adjusting the phase difference to compensate for the phase error in the quadrature combiner 180 as well as the amplitude errors in the IF_1 and IF_2 signal paths.

Figure 1D illustrates a plot of the image rejection calculated as a function of the total phase and amplitude error in an image-reject-mixer. The quadrature local oscillator (LO)

10 accuracy attained using most high-frequency I-Q signal generation techniques is on the order of < 1° resulting in a maximum image rejection on the order of ~ 40-50 dB. This assumes that an ideal IF quadrature combiner is available and that no quadrature LO phase tuning is performed.

To correct the phase and amplitude errors in an image-reject mixer, a test signal is

15 applied in the image band of the image-reject mixer and the image-reject mixer's internal parameters (such as gain and phase) are adjusted with the goal of maximizing the image-rejection attained.

There are many different implementations of the image-reject mixer and many different ways to calibrate such receiver architectures but most methods have a common

20 requirement. A test carrier is required to be present within the receive band of the transceiver for the purpose of detecting and eliminating the unwanted image signal through image-reject mixer calibration.

SUMMARY OF THE INVENTION

In accordance with the present invention, a differential two-or-more stage oscillator

25 with precision phase tuning is presented. The phase difference between the stages can be varied by differentially adjusting the propagation delays of each stage. In addition, an injection-locked differential two-or-more stage oscillator with precision phase tuning is presented. The phase relationship between the stages can be altered without altering the frequency of the oscillator by differentially altering bias input voltages coupled to each stage.

-4-

Because the oscillator is injection-locked, it is only necessary to vary one of the input voltages, with respect to the other, to vary the phase relationship between the stages.

Additionally, a mechanism for the realization of a self-calibrating image-reject mixer architecture within a radio transceiver utilizing the new oscillator circuits is introduced.

5   The foregoing is a summary and thus contains, by necessity, simplifications, generalizations and omissions of detail; consequently, those skilled in the art will appreciate that the summary is illustrative only and is not intended to be in any way limiting. As will also be apparent to one of skill in the art, the operations disclosed herein may be implemented in a number of ways, and such changes and modifications may be made without departing

10   from this invention and its broader aspects. Other aspects, inventive features, and advantages of the present invention, as defined solely by the claims, will become apparent in the non-limiting detailed description set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features

15   and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

Figure 1A, labeled prior art, illustrates a block diagram of a frequency halving circuit.

Figure 1B, labeled prior art, illustrates a conventional heterodyne receiver front end.

Figure 1C, labeled prior art, is a block diagram of an image reject mixer based on the

20   Hartley topology.

Figure 1D, labeled prior art, illustrates a graph of image rejection versus amplitude and phase errors in quadrature signals.

Figure 2 is a block diagram of a differential two-stage oscillator with variable quadrature output phases according to an embodiment of the present invention.

25   Figure 3 is a schematic diagram of the circuit of Figure 2 according to an embodiment of the present invention.

Figure 4 is a schematic of a differential regenerative frequency divider according to an embodiment of the present invention.

Figure 5 is a block diagram of an improved image reject mixer according to an embodiment of the present invention.

5   Figure 6 illustrates a flow diagram of image reject mixer operation according to an embodiment of the present invention.

Figure 7 illustrates a graph illustrating a typical image amplitude at IF versus phase or amplitude tuning control input.

Figure 8 illustrates a preferred embodiment of an image reject mixer calibration
10   method using tau-dither tracking.

Figure 9 illustrates waveforms associated with the tau-dither based image-reject calibration loop.

The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION
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The following is intended to provide a detailed description of an example of the invention and should not be taken to be limiting of the invention itself. Rather, any number of variations may fall within the scope of the invention that is defined in the claims following the description.

Introduction
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A differential two-or-more stage oscillator with precision phase tuning is presented. The phase difference between the stages can be varied by differentially adjusting the propagation delays of each stage. Differentially adjusting the propagation delays of each stage can be performed by creating any imbalance in the electrical symmetry of the stages,
25   for example, by differentially adjusting current sources coupled to each stage. In addition, an injection-locked differential two-or-more stage oscillator with precision phase tuning is presented. The phase relationship between the stages can be altered without altering the

frequency of the oscillator by differentially altering input voltages coupled to each stage. Because the oscillator is injection locked, it is only necessary to vary one of the input bias voltages, with respect to the other, to vary the phase relationship between the stages.

5   The presented phase tuning technique provides several important benefits. First, because the control mechanism for phase shifting is through a DC bias offset, it is relatively easy to make very small phase changes (on the order of < 0.1°) between the quadrature outputs of the ring. The smaller the DC offset, the smaller the phase change. Second, unlike the frequency-dependent phase shift found, for example, in an RC-network, the induced phase shift in the oscillator is strongly independent of the frequency of oscillation. This is

10   because the phase shift is a result of the difference between two frequency-dependent time delays in the ring. This implies that if a given phase shift is intentionally calibrated at one frequency, it does not need to be re-calibrated at other nearby frequencies.

       Additionally, a mechanism for the realization of a self-calibrating image-reject mixer architecture within a radio transceiver utilizing the new oscillator circuits is introduced. The

15   mechanism provides a practical means for allowing a portable wireless device, for example, a cellular telephone, to calibrate its internal receive and transmit image-reject-mixer's phase and amplitude errors without the use of an externally applied test signal. Specifically, the transmitting circuitry of a transceiver can be used to generate the test signals required to calibrate the image-reject-mixers in the receiver sections, and the receiver sections can be

20   used to calibrate the image-reject-mixers of the transmitter.

Precision Phase Tuning

       Figure 2 illustrates a differential two-stage oscillator 200 with precision phase tuning according to an embodiment of the present intention. Oscillator 200 includes a ring oscillator 221 and two current sources 228 and 230. Ring oscillator 221 includes a pair of differential

25   amplifiers 222 and 224 that are connected together as a ring oscillator. Propagation delay τ_A of amplifier 222 is controlled by varying the current of controllable current source 228. Propagation delay τ_B of amplifier 224 is controlled by varying the current of controllable current source 230. The oscillation frequency of ring oscillator 221 is inversely related to the total propagation delay ($\tau_A + \tau_B$) of amplifiers 222 and 224. Signal V_1 is measured across

30   nodes V_{1+} and V_{1-}. Signal V_2 is measured across nodes V_{2+} and V_{2-}.

799110 v3

If the propagation delays, τ_A and τ_B, of amplifiers 222 and 224 are equal, then signal V_2 will lag 90° behind signal V_1 (i.e. signals V_1 and V_2 will be quadrature signals). Propagation delay τ_A of amplifier 222 can be changed by adjusting the current of current source 228. Similarly, propagation delay τ_B of amplifier 224 can be changed by adjusting the

5   current of current source 230. The frequency of ring oscillator 221 can be varied without affecting the phase difference between signals V_1 and V_2 by adjusting the currents of current sources 228 and 230 proportionally. In addition, the phase difference between signals V_1 and V_2 can be varied by differentially adjusting the propagation delays, τ_A and τ_B, of amplifiers 222 and 224. Differentially adjusting the propagation delays can be performed by

10   differentially adjusting the currents of current sources 228 and 230.

Figure 3 is a schematic diagram of circuit 200 of Figure 2 according to an embodiment of the present invention. Amplifier 222 includes a pair of emitter coupled amplifiers Q_1 and Q_2. Amplifier 224 includes a pair of emitter coupled transistors Q_3 and Q_4. The collectors and bases of transistors $Q_1 - Q_4$ are connected to form ring oscillator 221. The

15   collectors of Q_1 and Q_2 are coupled to a voltage source V_{cc1} through resistors R_1 and R_2, respectively. The collectors of Q_3 and Q_4 are coupled to voltage source V_{cc2} through resistors R_3 and R_4 respectively.

Current source 228 includes a transistor Q_5. The base of transistor Q_5 is coupled to input voltage V_{bias1}, which controls the current of current source 228. Similarly, current

20   source 230 includes a transistor Q_6. The current of current source 230 is controlled by voltage signal V_{bias2}.

As the level of voltage signal V_{bias1} increases, the current of current source 228 increases causing an increase in the switching speed and a decrease in the propagation delay of differential amplifier 222. Similarly, the switching speed and propagation delay of

25   differential amplifier 224 are controlled by varying the level of voltage signal V_{bias2}.

Although the propagation delays of amplifiers 222 and 224 are described here as being controlled by varying the bias currents of the amplifiers (i.e. the currents of current sources 228 and 230), the same results can be attained by creating any imbalance in the electrical symmetry between amplifiers 222 and 224. For example, a bias voltage or current

30   can be altered at any node of ring oscillator 221. Alternatively, a controllable capacitor,

-8-

799110 v3

inductor or resistor can be coupled to any node to differentially alter the internal impedance of amplifier 222 with respect to amplifier 224.

In an alternate embodiment of the present invention, ring oscillator 221 can be implemented as a pair of quadrature coupled differential oscillators.

5   Figure 4 illustrates a differential regenerative (i.e. dynamic) divider 450 with quadrature output according to an embodiment of the present invention. Regenerative divider 450 is identical to circuit 200, except that the bases of transistors Q_5 and Q_6 are additionally coupled to an input signal V_{in} at nodes 452 and 454 through coupling capacitors Cc_1 and Cc_2.

Signal V_{in} is received at nodes 452, 454 and has a frequency f_{in}. Transistors Q_5 and

10   Q_6 convert input signal V_{in} into an alternating current signal i_{in} which is injected into emitter coupled nodes 456 and 458 of amplifiers 222 and 224. The frequency of current signal i_{in} is the same as the frequency f_{in} of input signal V_{in}. This injection locks ring oscillator 221 such that the oscillation frequency f_{osc} of the ring oscillator is half the input frequency f_{in} of input signal V_{in}.

15   If propagation delays τ_A and τ_B of amplifiers 222 and 224 are configured to be the same, then signals V_1 and V_2 are quadrature phased signals (i.e. they are separated in phase by 90°).

The phase relationship between V_1 and V_2 can be altered without altering the frequency of ring oscillator 221 by differentially altering input voltages V_{bias1} and V_{bias2}.

20   Because ring oscillator 221 is injection locked to frequency $f_{in}/2$, it is only necessary to vary one of the input voltages V_{bias1} or V_{bias2}, with respect to the other, to vary the phase relationship between V_1 and V_2.

In conventional circuits, the time delays through each stage of the ring oscillator are well-matched due to the electrical symmetry of the two stages of the quadrature ring. By

25   intentionally disrupting the symmetry of the ring, the time delay (or phase) through each stage of the ring is altered, resulting in a slight phase shift between the V_1 and V_2 outputs away from quadrature.

From a frequency-domain perspective, the frequencies of the higher order poles of each differential pair are sensitive to the transistor's bias current. By differentially altering

-9-

the bias current through each stage in the ring, the higher-order poles of each amplifier will shift in opposite directions, thus, intentionally altering the phase relationship between the quadrature outputs of the ring.

5   The presented phase tuning technique provides several important benefits. First, because the control mechanism for phase shifting is through a DC bias offset, it is relatively easy to make very small phase changes (on the order of < 0.1°) between the quadrature outputs of the ring. The smaller the DC offset, the smaller the phase change. Second, unlike the frequency-dependent phase shift found, for example, in an RC-network, the induced phase shift in the oscillator is strongly independent of the frequency of oscillation. This is

10   because the phase shift is a result of the difference between two frequency-dependent time delays in the ring. This implies that if a given phase shift is intentionally calibrated at one frequency, it does not need to be re-calibrated at other nearby frequencies.

Self Calibration of An Image Reject Mixer

       A mechanism for the realization of a self calibrating image-reject mixer architecture

15   within a radio transceiver is introduced. The mechanism provides a practical means for allowing a portable wireless device (such as a cellular telephone) to calibrate its internal receive and transmit image-reject-mixer's phase and amplitude errors without the use of an externally applied test signal. Specifically, the transmitting circuitry (or sub-blocks) of a transceiver can be used to generate the test signals required to calibrate the image-reject-

20   mixers in the receiver sections (or circuit-blocks), and the receiver sections can be used to calibrate the image-reject-mixers of the transmitter.

       The frequency halving circuits (I-Q generator) with phase tuning as illustrated in Figures 2, 3, and 4, can be utilized to finely adjust the quadrature LO phases according to the present invention. This phase tuning ability enables the systematic offset in an image-reject-

25   mixer to be removed, thereby maximizing image-rejection of the receiver.

       According to the present invention, a test carrier can be generated by the transmitter section of a transceiver and can be internally coupled to the receiver section of the same radio transceiver for the purpose of calibrating the image-reject mixer section of the receiver or an image-reject mixer section of the transmitter. A received signal strength indicator circuit

30   (which is found in most modern receiver systems) can be used to detect and measure the

-10-

magnitude of the undesired image signal present at the output of the image-reject mixer. This information can then be used to provide the feedback information required for the calibration of the image-reject mixer. The goal of the calibration is to maximize rejection of the image carrier by compensating for phase and amplitude errors in the I and Q image reject mixer

5   paths either in the RF (input radio-frequency), LO (local oscillator), or IF (intermediate frequency) paths. This includes in a digital domain if a digital IF section is used which has as inputs the I and Q IF signals from the front-end of the image-reject mixer architecture.

Conventional radio transceivers do not tune the output frequency of their own transmit section to generate a test signal in the image-band of the receiver for the purpose of

10   calibrating the image-reject mixer of the receiver. In addition, conventional radio transceivers do not use their own receiver to detect the signal strength of the unwanted image carrier generated by the transmitter section for the purposes of calibrating out the phase and amplitude errors in the transmitter's image-reject mixer. A goal of the present invention is to reduce image-signal generation of the transmit section. Thus the image-reject mixer to be

15   calibrated can lie in either the receive section, the transmitter section or there can be an image-reject mixer in both sections to be calibrated.
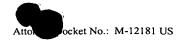
When a receiver's image-reject mixer calibration requires a test signal to be generated within the image-band of the receiver (ideally at an offset from the first LO equal to the IF output of the image-reject mixer), the test source needs to be generated at a fixed frequency.

20   Thus, the transmit section can be an effective source for the test signal because in most high performance radios, a transmit section is required to be capable of synthesizing a precision frequency output in normal operation.

An alternative source for a precision frequency test signal is from the reference oscillator source used in the frequency synthesizer of a transceiver, or from the precision

25   clock signal used to synchronize the digital logic or data circuitry of a transceiver. Both of these high precision sources are very often found in the tens of MHz region, typically far below the required frequency of the test image signal (which can be in the GHz range or on the order of a decade higher). The waveform of the digital clocking or reference source can be altered from that of a pure sine-wave by clipping or limiting the amplitude of the signal.

30   This allows higher order harmonics found at integer multiples of the fundamental frequency of the signal. The low levels of these high harmonics is actually a desirable feature due to the

-11-

high sensitivity of the low noise amplifier which usually precedes the image-reject mixer in a receiver architecture. The synthesizer frequency of the first LO of the receiver can then be selected such that one of the harmonics of the clock or reference falls at the image frequency of the receiver while no harmonic falls at the desired RF input frequency of the receiver. The harmonic found at the image will then (by proper selection of LO frequency) get converted to the IF as a useful test carrier to calibrate the image rejection of the receiver.

One benefit of the present invention is that the transmitter circuit or test signal generating source is isolated from the antenna of the transceiver such that the test signal is prevented from radiating to the outside world during the calibration. This can be accomplished by any means of breaking the RF path from the transmitter to the external radiating antenna, or by shunting that path to a ground potential. The RF path from the external antenna to the receiver is also broken (or shunted to ground) so that the receiver does not pick up external radio signals from it's antenna during the calibration.

Figure 5 shows an improved image reject mixer 500 according to embodiments of the present invention. Components of image reject mixer 500 that correspond to components of image reject mixer 170 of Figure 1C are identified by the same reference numerals. Signal generator 171 has been replaced with circuit 450 of Figure 4. Nodes 452 and 454 of circuit 450 are coupled to a signal generator 502.

Output signal IF_{out} is received by a carrier level detector 503. Carrier level detector 503 provides a signal to feedback controller 504. Feedback controller 504 provides control signals to switches SW_1 and SW_2, calibration signal transmitter 506, signal generator 502, amplifiers 510 and 512, and provides voltage signals V_{bias1} and V_{bias2}.

Figure 6 illustrates a flow diagram of image reject mixer 500 operation according to an embodiment of the present invention. Image reject mixer 500 has a calibration mode 602 and an operation mode 604.

Initially, in calibration mode 602, controller 504 sets several configurations, step 610. Setting configurations include (a) configuring switches SW_1 and SW_2 to connect calibration signal transmitter 506 to input node RF_{in}; (b) configuring signal generator 502 to produce a signal with a frequency twice that required for the local oscillator signals V_1 and V_2; (c) configuring voltage signals V_{bias1} and V_{bias2} to initiate the operation of circuit 450 with the

-12-

phase delays of amplifiers 222 and 224 being approximately equal; (d) configuring calibration signal transmitter 506 to generate a signal at the frequency of the image; and (e) setting the gains of amplifiers 510 and 512 equal.

5   Controller 504 then runs a calibration algorithm, step 620. Signal IF_{out} is generated as in image reject mixer 170, sub-step 622. Signal IF_{out} contains the image signal generated by calibration signal generator 506. The level of signal IF_{out} corresponds to phase and amplitude errors introduced in quadrature combiner 180 and other components of image reject mixer 500. Carrier level detector 503 provides a signal corresponding to the level of signal IF_{out} to controller 504, sub-step 624.

10   Controller 504 then adjusts the relative propagation delays of amplifier 222 and 224 (within circuit 450) to control the relative phase difference between V_1 and V_2 to reduce the signal level of IF_{out} as much as possible, sub-step 626. Controller 504 then adjusts the relative gains of amplifiers 510 and 512 to reduce the signal level of IF_{out} as much as possible, sub-step 628. Controller 504 then alternately attempts to reduce the signal level of 15 IF_{out} by adjusting the phase difference between V_1 and V_2 and by adjusting the relative gains of amplifiers 510 and 512, sub-step 630. When no further reduction of IF_{out} is attained for several iterations, calibration mode 602 is terminated by configuring switches SW_1 and SW_2 to disconnect the calibration signal transmitter 506 from node RF_{in} and to connect the antenna to node RF_{in}, step 640.

20   Image reject mixer 500 then enters operation mode 604. The setting for the phase difference between V_1 and V_2 and the relative gains of amplifiers 510 and 512 determined during the calibration mode are retained during the operation mode to maintain the improved image reject performance of image reject mixer 500 attained during calibration mode.

         Image reject mixer 500 can be integrated. The functionality of the elements of image 25 reject mixer 500 contained within dashed boundary 516 may wholly or partially implemented using analog or digital technology.

         In addition, image reject mixer 500 can be used with a transmitter.

         There are many types of error minimization algorithms (both analog and digitally based schemes) which can be used to correct the phase and amplitude of the fixed offset 30 errors of an image-reject mixer. A manual form of an algorithm would be to inject a test

-13-

799110 v3

signal at the image frequency of the receiver and to observe the signal amplitude of the image in the IF output. The phase angle between the I and Q LO signals is then adjusted for maximum image rejection (or minimum IF signal magnitude). Next the gain between the I and Q paths of the image-reject mixer are tuned to find a new maximum image rejection.

5   Ideally there should be no need to go back and readjust the phase angle, but in a practical system, phase and gain controls are not quite independent. With a few iterations back and forth between adjusting phase and then the gain, the performance of the image-reject mixer can be drastically improved.

An analog technique which is well suited to correct the phase and gain offset errors in

10   a transceiver application, is based on the Tau-Dither minimization technique as presented in *"Spread spectrum systems with commercial applications,"* R. C. Dixon, 3rd ed., New York NY: John Wiley & Sons, Inc., 1994, pp. 254-259.

Figure 7 illustrates a typical curve of the test image signal amplitude as a function of phase correction or amplitude correction control signals. It can be seen that in the portion of

15   the curve marked as section 2, the image-signal amplitude reaches a minimum value. Note that the minimum value of image signal amplitude at IF corresponds to a maximum image rejection goal for the calibration.

Assume that a phase offset error in the image-reject mixer is calibrated out first. A test carrier is input to the image-reject mixer at the image frequency of the receiver. Suppose

20   the image signal amplitude at the IF output of the image-reject mixer is found to be at the point marked as "a" in section 1 of the curve in Figure 7. By increasing and decreasing (or dithering) the phase tuning control signal between points a and b, the image signal amplitude increases and decreases in a way which indicates the correct direction of optimization. In section 2 of the curve, dithering the control value between points a and b does not give rise to

25   any directional indication and thus the control signal is at the optimum value for minimized image signal.

Figure 8 illustrates a preferred embodiment of a calibration loop employing Tau-Dither tracking to calibrate out the phase and amplitude offset errors in an image reject mixer. Many of the annotated nodes of Figure 8 are plotted in Figure 9 as a function of the

30   waveform of interest, the section of the curve of Figure 7 within which the operation is described, and as a function of time (along the x-axis of each sub-plot in the figure).

-14-

The image-reject (IR) mixer block 800 is an image-reject receiver architecture (commonly a Hartley or Weaver topology), and may be implemented using analog or digital circuit techniques or a combination of both. Upon beginning calibration, a system controller 808 first isolates the transceiver's antenna port from the RF input port of IR mixer block 800 and from a test signal generator block 812 through an antenna isolation circuit function 812. Antenna isolation circuit function 812 prevents external RF signals from coupling to the input (RF in) of the IR mixer during calibration, and prevents unintentional radiation of the signal from a test signal generator block 811 out through the antenna. Test signal generator block 811 is designed to generate a signal frequency precisely at the image frequency of the IR mixer. System controller 808 can adjust the IR mixer's receive frequency through a control input, and can also have the flexibility of controlling the transmitting frequency of test signal generator 811. In one embodiment, the transmitter or up-converter of a transceiver is used to perform the required functions of test signal generator block 811. Once the test signal frequency and receive frequency of IR mixer 800 are selected such that the test signal frequency falls at the image frequency of the IR mixer 800, the unwanted image carrier will be present at the IF (intermediate frequency) output of IR mixer 800. To begin correcting the phase errors in IR mixer 800, system controller 808 instructs a track and hold function 809 to go into track mode and pass the calibration control voltage directly through to the I-Q phase angle control input. Low frequency oscillator 804 is designed to generate a low frequency dither signal (see V_{LFO} in Figure 9) which is summed through block 907, directly to the "calibration control voltage" node and hence into the I-Q phase angle control node during phase calibration. This low frequency signal acts to dither the phase control between two nearby values (marked as "a" and "b" in Figure 7).

Figure 9 illustrates three key sections on the image signal amplitude versus control value curve. Calibration will typically begin with the calibration control voltage at a non-optimum value (either too high or too low). If at the beginning of calibration the phase error lies in section 1 of the curve, the waveforms under the heading "Section 1" in Figure 9 describe the signal waveforms within the calibration loop. Beginning with the output of low frequency oscillator (LFO) 804, the V_{LFO} timing diagram in row 'iv' shows that block 804 generates a square wave type signal. Due to the negative sign in the summation function 807, a negative (starting) value for V_{LFO} results in an increase in the calibration control voltage to the point "b" in section 1 of Figure 7. Half a V_{LFO} period later, the control voltage is

-15-

799110 v3

decreased a step to point "a" in Section 1 of Figure 7. At point "b", the amplitude of the test carrier which appears at the IF output of block 800 is smaller than at point "a". Since the period of the V_{LFO} is by design much larger than the IF period, only the envelope of the IF signal can be observed in the V_{IF} timing diagram (row "i") of Figure 9. The amplitude of the IF signal can be clearly seen to follow the polarity of the V_{LFO} signal as expected in Section 1 of Figure 7. Note that the markings of "a" and "b" on the V_{LFO} timing diagrams of Figure 9 do not represent the V_{LFO} voltage value but are simply markers to identify the corresponding position on Figure 7 for a given value of V_{LFO}.

Circuit block 801 extracts the amplitude (or envelope) information from the IF carrier (V_{IF}). This can be done using a simple envelope detection circuit, or an AM demodulator, or the Received Signal Strength Indicator (RSSI) of a receiver which is designed to accurately measure signal power at the IF. The timing diagram labeled V_{ENV} (row "ii" in Figure 9) shows the required output signal from block 801. Block 802 is then employed to remove the dc content from this signal V_{ENV} and any other frequency content which is not near the frequency of the LFO 804. The timing diagram V_{AM} in Figure 9 illustrates the output from block 802 if it is realized using a band pass filter designed to pass only the fundamental harmonic of the LFO frequency.

The V_{AM} signal is then multiplied with the V_{LFO} using an analog multiplier (block 803) to generate signal V_M. Figure 9 clearly shows that the V_M signal will have a positive dc component. This dc component is extracted through the use of block 805 (which can be implemented with a low pass filter). This dc signal V_E, is a negative feedback error signal which is proportional to the negative of the slope of the curve of Figure 7. Notice a positive value of V_E is observed in timing diagram row "vi" in the column of "Section 1" in Figure 9. The polarity of the signal indicates the correct direction in which the average Calibration Control Voltage should move in order to minimize the image signal amplitude in the IF and thus improve the image rejection of the IR mixer block 800. Block 806 integrates signal VE and adds it to the Calibration Control Voltage node to close the feedback loop of the calibration circuit. The integrator will integrate the positive value of VE and slowly increase the calibration voltage while the incremental dithering by the V_{LFO} continues. The timing diagrams in Figure 9 clearly illustrate how in "Section 3" of the curve of Figure 7 the polarity of V_E will result in a negative value. In this case, the integrator will then correctly decrease the average value of the calibration control voltage and head towards Section 2 of Figure 7.

-16-

At the minimum point in the IF image amplitude versus control signal curve (i.e. Section 2 in Figure 7), V_E is shown to be zero and therefore the calibration control voltage is at the optimum value for maximum image rejection. Once controller 808 decides to end calibration, the calibration control voltage which (during this hypothetical phase calibration)

5   was being passed through or tracked by block 809 is then held by block 809 through a functional control command from the controller. In this way, the calibrated value is stored and kept as input to the IR mixer block so that the mixer block retains the superior image-rejection performance achieved through the calibration.

With the phase calibration complete, the controller can then place block 810 in track

10   mode and thus calibrate the gain balance of the IR mixer block. With a few iterations between gain calibration and phase calibration, a final maximum-image rejection performance will be obtained using this technique.

Once both gain and phase calibrations are finally complete, both blocks 809 and 810 are kept in hold mode for the duration of required operation of the IR mixer (block 800).

15   Test signal generator (block 811) is no longer required and can be disengaged. The antenna can now be re-coupled to the RF input port of the IR mixer in order to use the IR mixer as a receiver for receiving radio signals through the antenna.

A similar feedback loop can be used to calibrate the image-rejection of the transmit section of a transceiver. The antenna is once again isolated from the transceiver to prevent

20   unintentional signal reception or transmission and the IR mixer of the receiver (800) is set to receive (in it's non-image band), the image carrier of the transmit IR up-converting mixer (not illustrated but can be considered as similar to 800). The frequencies for the transmitter and receiver during calibration are chosen such that only the image carrier of the transmitter will fall in the IF of the receiver and thus be demodulated by block 801 of the receiver

25   section. The calibration loop then works exactly the same way except that the calibration control voltage is also connected to other track and hold blocks which feed the phase control and gain balance control adjustment inputs to the transmitter's up converting IR mixer (not illustrated in Figure 8).

Calibration proceeds in the same way as described before so that the phase and gain

30   tuning correction voltages can be stored in the transmitter's IR mixer's equivalent track and

-17-

hold blocks. Once both the transmitter and receiver have been calibrated, then the antenna isolation is removed and normal radio operation may begin.

5   Other embodiments are within the following claims. Also, while particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the appended claims are to encompass within their scope all such changes and modifications as fall within the true spirit and scope of this invention.

799110 v3